This listing of the claims will replace all prior versions, and listings, of claims in the present application:

LISTING OF CLAIMS:

Claims 1-20 (Cancelled).

Claim 21 (Currently Amended) A semiconductor structure comprising:

~~at least one~~ a first semiconductor active area having, and laterally surrounded by, a first sidewall and located in a semiconductor substrate;

~~with~~ a first trench isolation region ~~and~~ laterally abutting said [[a]] first sidewall ~~between said first semiconductor area and said first trench isolation region, wherein said first trench isolation region~~ and surround[[s]]ing said first semiconductor active area and compris[[es]]ing silicon oxide, wherein [[and]] said first sidewall ~~is void of~~ does not contact any nitride liner; [[and]]

~~at least one~~ a second semiconductor active area having, and laterally surrounded by, a second sidewall and located in said semiconductor substrate;

a nitride liner laterally abutting said second sidewall; and

~~with~~ a second trench isolation region ~~and~~ laterally abutting said nitride liner ~~a second sidewall between said second semiconductor area and said second trench isolation region, wherein said second trench isolation region~~ and surround[[s]]ing said second semiconductor active area and compris[[es]]ing silicon oxide ~~and a nitride liner is present on said second sidewall~~.

Claim 22 (Currently Amended) The semiconductor structure of Claim 21, wherein said first semiconductor active area is under a first compression stress and said second semiconductor active area is under a second compression stress and the level of first compression stress is higher than the level of second compression stress.

Claim 23 (Currently Amended) The semiconductor structure of Claim 21, wherein said nitride liner is present on the entirety of said second sidewall surrounding said second semiconductor active area~~layer~~.

Claim 24 (Currently Amended) The semiconductor structure of Claim 21, wherein ~~substantially no~~ any bird's beak structure comprising a dielectric material and having a taper in lateral width is ~~present~~ absent between said first semiconductor active area and said first trench isolation region.

Claim 25 (Currently Amended) The semiconductor structure of Claim 21, further comprising ~~wherein~~ at least one bird's beak structure including a dielectric material and having a taper in lateral width and located ~~is present~~ between said second semiconductor active area and said second trench isolation region.

Claim 26 (Currently Amended) The semiconductor structure of Claim 21, ~~wherein substantially no bird's beak structure is present between said first semiconductor area and said first trench isolation region and~~ further comprising at least one bird's beak structure comprising a dielectric material and having a taper in lateral width and located ~~is present~~ between said second

semiconductor active area and said second trench isolation region [[.]], wherein any bird's beak structure comprising a dielectric material and having a taper in lateral width is absent between said first semiconductor active area and said first trench isolation region.

Claim 27 (Currently Amended) The semiconductor structure of Clam 21, wherein said first semiconductor active area includes at least one PFET and said second semiconductor active area includes at least one NFET.

Claim 28 (Cancelled).

Claim 29 (Previously Presented) The semiconductor structure of Claim 21, wherein said nitride liner is a nitride surface layer that has a thickness of about 0.1 nm to about 2.0 nm.

Claim 30 (Previously Presented) The semiconductor structure of Claim 21, wherein a nitride liner is present on at least a portion of a bottom of said first trench isolation region.

Claim 31 (Previously Presented) The semiconductor structure of Claim 21, wherein at least a portion of a bottom of said second trench isolation region is void of any nitride liner.

Claim 32 (Currently Amended) A semiconductor structure comprising:

a trench isolation region located in a semiconductor substrate;

~~at least one~~ a first semiconductor active area having, and laterally surrounded by,[[with]] a first sidewall that ~~adjoins~~ laterally abuts said trench isolation region and is located in said semiconductor substrate, wherein said first sidewall does not contact any nitride liner; [[and]]

~~at least one~~ a second semiconductor active area having, and laterally surrounded by,[[with]] a second sidewall ~~that adjoins said trench isolation region~~ and located in said semiconductor substrate; and

a nitride liner laterally abutting said second sidewall and said trench isolation region ~~wherein said first sidewall is void of any nitride liner and a nitride liner is present on said second sidewall~~.

Claim 33 (Currently Amended) The semiconductor structure of Claim 32, wherein said first semiconductor active area is under a first compression stress and said second semiconductor active area is under a second compression stress and the level of first compression stress is higher than the level of second compression stress.

Claim 34 (Previously Presented) The semiconductor structure of Claim 32, wherein the entirety of said first sidewall is void of any nitride liner and said nitride liner is present on the entirety of said second sidewall.

Claim 35 (Currently Amended) The semiconductor structure of Claim 32, wherein ~~substantially no~~ any bird's beak structure including a dielectric material and having a taper in lateral width is ~~present~~ absent between said first semiconductor active area and said first trench isolation region.

Claim 36 (Currently Amended) The semiconductor structure of Claim 32, further comprising ~~wherein~~ at least one bird's beak structure including a dielectric material and having a taper in lateral width and is located ~~is present~~ between said second semiconductor active area and said second trench isolation region.

Claim 37 (Currently Amended) The semiconductor structure of Clam 32, wherein said first semiconductor active area includes at least one PFET and said second semiconductor active area includes at least one NFET.

Claim 38 (Cancelled).

Claim 39 (Previously Presented) The semiconductor structure of Claim 32, wherein said nitride liner is a nitrided surface layer that has a thickness of about 0.1 nm to about 2.0 nm.

Claim 40 (Previously Presented) The semiconductor structure of Claim 32, wherein said first sidewall does not adjoin said second sidewall.